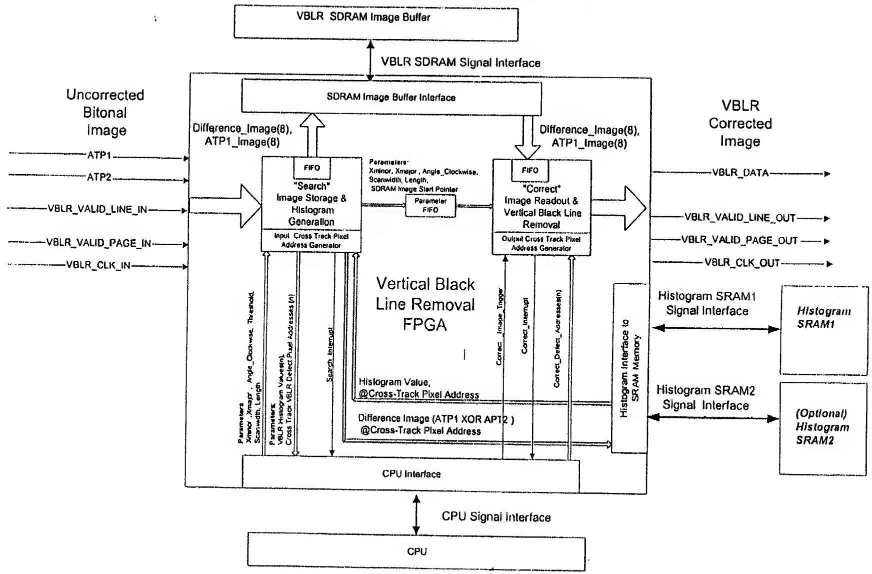

VBLR SDRAM Image Buffer
VBLR SDRAM Signal Interface
SDRAM Image Buffer Interface
Uncorrected Bitonal Image
ATP1
ATP2
VBLR_VALID_LINE_IN
VBLR_VALID_PAGE_IN
VBLR_CLK_IN
Difference_Image(8), ATP1_Image(8)
FIFO
"Search" Image Storage & Histogram Generation
Input Cross Track Pixel Address Generator
Parameters: Xminor, Xmajor, Angle_Clockwise, Scanwidth, Length, SDRAM Image Start Pointer
Parameter FIFO
Difference_Image(8), ATP1_Image(8)
FIFO
"Correct" Image Readout & Vertical Black Line Removal
Output Cross Track Pixel Address Generator
VBLR Corrected Image
VBLR_DATA
VBLR_VALID_LINE_OUT
VBLR_VALID_PAGE_OUT
VBLR_CLK_OUT
Vertical Black Line Removal FPGA
Parameters Xminor, Xmajor, Angle_Clockwise, Threshold, Scanwidth, Length
Parameters VBLR Histogram Values(n), Cross Track VBLR Defect Pixel Addresses (n)
Search_Interrupt
Histogram Value, @Cross-Track Pixel Address
Difference Image (ATP1 XOR APT2) @Cross-Track Pixel Address
Correct_Image_Trigger
Correct_Interrupt
Correct_Defect_Addresses(n)
Histogram Interface to SRAM Memory
Histogram SRAM1 Signal Interface
Histogram SRAM1
Histogram SRAM2 Signal Interface
(Optional) Histogram SRAM2
CPU Interface
CPU Signal Interface
CPU

Figure 1

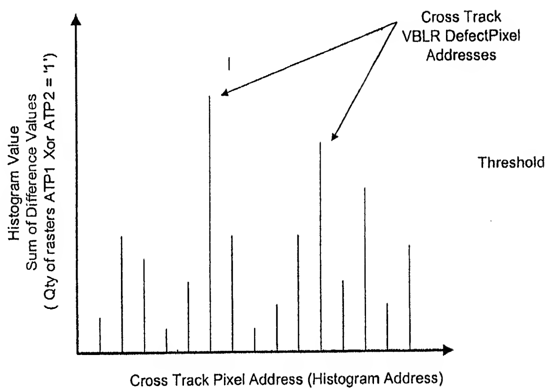

Histogram Value
Sum of Difference Values
(Qty of rasters ATP1 Xor ATP2 = '1')
Cross Track
VBLR DefectPixel
Addresses
Threshold
Cross Track Pixel Address (Histogram Address)

Figure 2

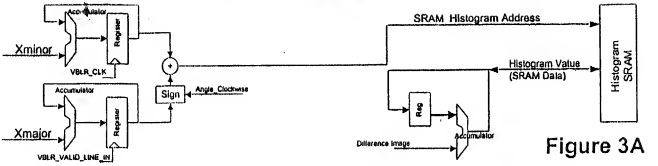


Figure 3A

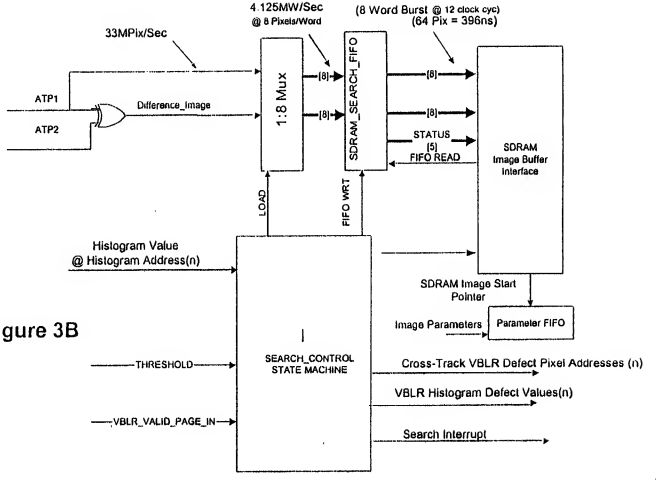


Figure 3B

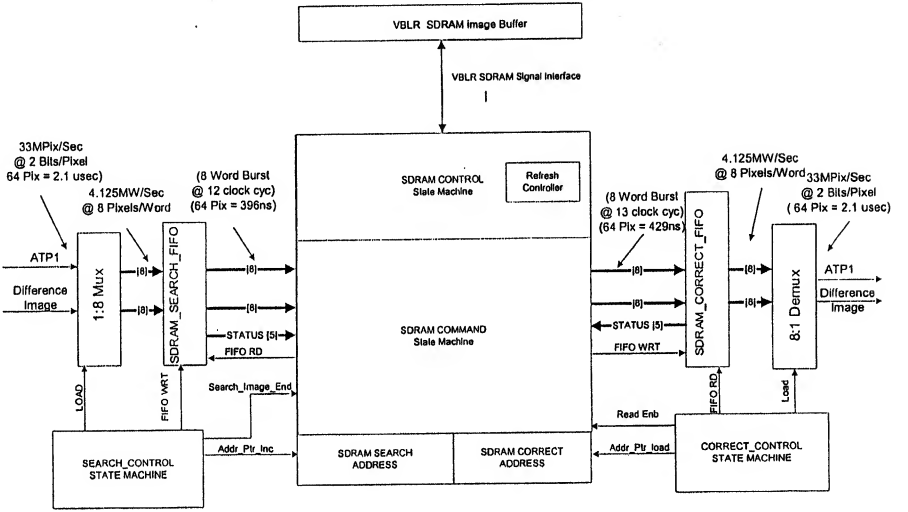
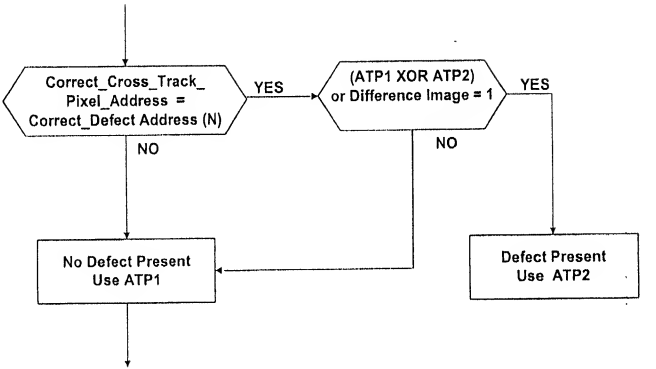


Figure 4

Figure 5


Correct_Cross_Track_
Pixel_Address =
Correct_Defect Address (N)
YES
(ATP1 XOR ATP2)
or Difference Image = 1
YES
NO
NO
No Defect Present
Use ATP1
Defect Present
Use ATP2

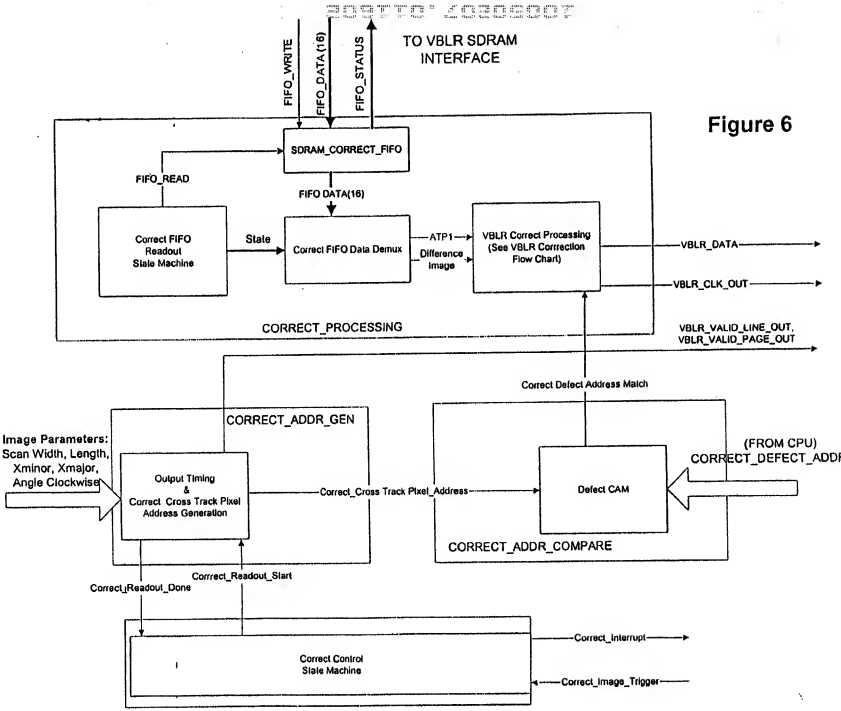


Figure 6